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a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material on the titanium aluminide layer, said conductive material and said titanium aluminide layer being in contact at an interface, said interface being substantially free from tensile stress between said titanium aluminide layer and said conductive material.

27. (Three Times Amended) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

28. (Three Times Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over said second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer on the titanium aluminide layer and in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer on the titanium aluminide layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer over the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material on the titanium aluminide layer, wherein said conductive material and said titanium aluminide layer are in contact at an interface having approximately no tensile stress from said titanium aluminide layer; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

35. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer over the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer on the titanium aluminide layer at a contact interface, wherein said contact interface experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer over the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer over the metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material on the titanium aluminide liner, wherein said conductive material is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said conductive material.

39. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer over the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.